DC AND RF TECHNIQUES FOR COMPUTING ACCESS RESISTANCES IN MICROWAVE FET's

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ABSTRACT

In order to estimate the access resistances of PHEMTs two different techniques based on *I(V)* and RF measurements were investigated. An improved cold-FET technique is presented. The main difference between the classical and the proposed cold-FET techniques lies on the open circuit condition in drain-source instead of short circuit condition (V_{DS}=0 V). A good agreement is observed between the values of parasitic resistances computed from DC *I(V)* and RF measurements.

I. INTRODUCTION

PHEMTs equivalent circuit can be represented by merging the intrinsic transistor elements into the extrinsic device elements. The basic cell for linear, non-linear and noise models is the intrinsic transistor. The element values of the intrinsic transistor can be obtained by de-embedding the extrinsic elements. A good extraction of extrinsic device elements leads to the true values of the intrinsic transistor, therefore to good models. Extrinsic elements and particularly access resistances, i.e. source, drain and gate resistances R_S, R_D and R_G respectively, are very difficult to extract from electrical measurements. In the past, different techniques based on DC and RF measurements [1, 2, 3] have been proposed to estimate these resistances. The main problem up to now is that results computed from both kinds of techniques are not consistent with each other. The purpose of this paper is firstly, to explain why DC an RF techniques for access resistances estimation have led to different results, and secondly, to give the conditions under which both techniques are consistent with each other. DC and RF methods for computing access resistances are described and then the main results supporting the compatibility of both methods are presented.

II. DC METHOD

A. The planar Schottky diode model

The planar Schottky diode formed by gate-source or gate-drain contacts is modeled by the circuit indicated in fig. 1. Under forward bias condition, for any positive value of V_G, the current I_G flowing through the circuit of fig. 1 is computed by:

$$I_G = I_S \cdot \exp\left(\frac{V_G - RI_G}{nU_T}\right) \quad (1)$$

where: I_S is the saturation current (A); R is the series resistance associated to the real Schottky diode; n is the ideality factor of the diode; U_T is the thermal potential (V) where $U_T = kT/q$; k is the Boltzman constant (J/K); T is the absolute temperature (K); q is the electron charge (C). The saturation current is given by:

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$$I_S = S \cdot A^* \cdot T^2 \cdot \exp\left(\frac{-\Phi_{bi}}{U_T}\right) \quad (2)$$

where: S is the gate surface (cm^2); A^* is the Richardson constant ($Am^{-2}K^{-2}$); Φ_{bi} is the Scottky barrier (V). From equation (1) the expression of V_G versus I_G is derived:

$$V_G = R\,I_G + nU_T \ln(I_G) - nU_T \ln(I_S) \quad (3)$$

At drain or source floating respectively, V_G is equal to V_{GS} or V_{GD}, R is equal to $R^{(S)}$ or $R^{(D)}$, I_G is equal to I_{GS} or I_{GD}, and n is equal to n_S or n_D. Moreover, for a transistor the values of the series resistance R can be written as [1]:

$$R^{(S)} = R_S + R_G + \frac{R_{CH}}{3} \quad (4)$$

$$R^{(D)} = R_D + R_G + \frac{R_{CH}}{3} \quad (5)$$

where: R_{CH} is the channel resistance. Based on (m) measurements of $I_{GS}(V_{GS})$ or $I_{GD}(V_{GD})$ at drain or source floating respectively, a least squares optimization method [4] is used for computing the coefficients of equation (3), among which there is the series resistance $R^{(S)}$ or $R^{(D)}$. This method consists on the determination of the minimum of the function $X(R, a, b)$ defined as:

$$X = \sum_{i=1}^{m}\left(R\,I_{Gi} + a\ln(I_{Gi}) + b - V_{Gi}\right)^2 \quad (6)$$

where: $a = nU_T$ and $b = -a\ln(I_S)$. The minimum of X occurs when the partial derivatives with respect to R, a and b are equal to zero. These conditions lead to the resolution of three simultaneous linear equations where R, a and b are the unknowns.

B. The R^{end} technique

Apart from equations (4) and (5), other access resistance terms can be defined using non-gate voltages [1]:

$$R_S^{end} = \left(\frac{V_{DS}}{I_{GS}}\right) = R_S + \frac{R_{CH}}{2} \quad \text{drain open} \quad (7)$$

$$R_D^{end} = \left(\frac{V_{SD}}{I_{GD}}\right) = R_D + \frac{R_{CH}}{2} \quad \text{source open} \quad (8)$$

where V_{DS} is the drain-source voltage, V_{SD} is the source-drain voltage, both measured at drain or source floating.

III. RF METHOD

This method uses **Z** parameters computed from the measurement versus frequency of **S** parameters at $V_{GS} > V_{bi} > 0$ and at drain open for different I_{GS} currents. At $V_{GS} > V_{bi} > 0$ the PHEMT equivalent circuit is reduced to the circuit shown in Fig. 2. At low frequencies ($f < 10$ GHz) the influence of C_{pg} and C_{pd} on **Z** parameters can be neglected. Under these conditions **Z** parameters of circuit on fig. 2 are given by:

$$\mathbf{Z} = \begin{bmatrix} R_S + R_G + \frac{R_{CH}}{3} + Z_D + jw(L_S + L_G) & R_S + \frac{R_{CH}}{2} + jwL_S \\ R_S + \frac{R_{CH}}{2} + jwL_S & R_S + R_D + R_{CH} + jw(L_S + L_D) \end{bmatrix} \quad (9)$$

where $Z_D = \frac{n_S kT}{qI_{GS}}$.

It is noticed that imaginary parts of **Z** parameters are directly related to parasitic inductances L_S, L_D and L_G, while real parts, except for Z_{11} parameter, are directly related to access resistances. Regarding $\mathrm{Re}(Z_{11})$, the extraction of access resistances terms is achieved considering that the plot of $\mathrm{Re}(Z_{11})$ versus $1/I_{GS}$ is a straight line where the slope is equal to $n_S kT/q$ and the y-axis intercept corresponds to the access resistances terms.

IV. RESULTS AND CONCLUSIONS

S parameter measurements in the frequency range .045-20 GHz were performed on a PHEMT (NE24200) with a network analizer HP8510C at the bias condition

$V_{GS} > V_{bi} > 0$ and at drain floating (open circuit condition) for different gate currents 6 mA < I_{GS} < 7 mA. Prior to S parameter measurements a TRL calibration was carried out on the network analizer (TRL for on test-fixture measurements). Values of different access resistances terms and other physical parameters computed from DC and RF measurements are gathered in Table I. As for DC measurements, Fig. 3 shows the curves of $I_{GS}(V_{GS})$ and $I_{GD}(V_{GD})$ at drain or source floating respectively, and Fig. 4 shows the curves of $I_{GS}(V_{DS})$ and $I_{GD}(V_{SD})$ at drain or source floating respectively. Concerning RF measurements, the variations of Re(Z_{ij}) against frequency at drain floating are plotted in Fig. 5. It should be noted that in the frequency range .045 Ghz $\leq f \leq$ 10 GHz real parts of Z_{11}, $Z_{12}=Z_{21}$ and Z_{22} are constant, as predicted by the theory. Parasitic resistances terms ($R_S+R_{CH}/2$) and ($R_S+R_D+R_{CH}$) are computed from Re(Z_{12}) and Re(Z_{22}) in this frequency range. In addition, the plot of Re(Z_{11}) versus $1/I_{GS}$ at drain floating, reported on Fig. 6, is a straight line as expected by the theory. Other access resistance terms reported on Table I are obtained by linear combinations of the computed access resistance terms. Values gathered on Table I indicate a good agreement between DC and RF techniques. So, full extraction of the equivalent circuit model can be achieved with RF measurements only. Finally, it should be noted that forward gate currents used in our experiments are not as high as to degrade the transistor [3].

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REFERENCES

[1] S. Chaudhuri and M. B. Das, "An investigation of MESFET "end" resistance using a distributed diode/resistance model," *IEEE Trans. on Electron Devices*, vol. ED-32, No. 11, pp. 2262-2268, Nov. 1985.

[2] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rodhe, "A new and reliable direct parasitic extraction method for MESFETs and HEMTs," *23rd European Microwave Conference*, pp. 451-453, 1993.

[3] B. S. Kim and S. Nam "An iterative parasitic extraction method for HEMT," *25th European Microwave Conference*, pp. 558-561, 1995.

[4] R. J. Bennett, "Interpretation of forward bias of Schottky barriers," *IEEE Trans. on Electron Devices*, vol. ED-32, No. 11, pp. 935-937, April 1987.

PARAMETER	DC MODEL	RF MODEL
$R_S+R_{CH}/2$ (Ω)	2.17	2.08
$R_D+R_{CH}/2$ (Ω)	2.37	2.30
$R_S+R_D+R_{CH}$ (Ω)	4.54	4.40
$R_S+R_G+R_{CH}/3$ (Ω)	3.87	3.73
$R_D+R_G+R_{CH}/3$ (Ω)	4.10	
$R_G-R_{CH}/6$ (Ω)	1.70	1.65
n_S	1.57	1.53
n_D	1.56	
I_{GD} (A)	$3.87.10^{-12}$	
I_{GS} (A)	$3.65.10^{-12}$	

Table I. Comparison of DC and RF techniques for access resistances estimation.

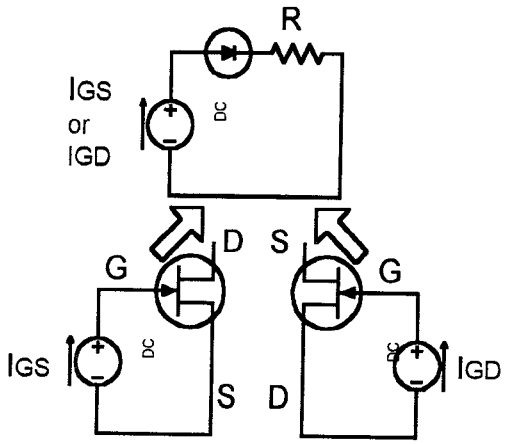

Fig. 1 Equivalent circuit of transistor with drain or source floating.

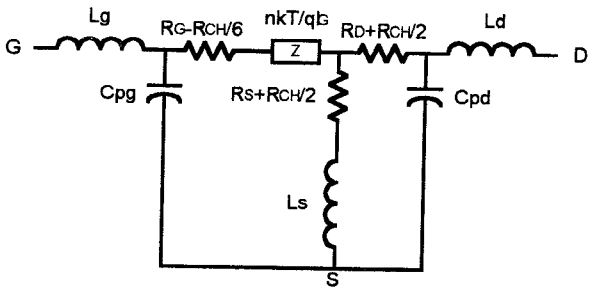

Fig. 2 Equivalent circuit of transistor at drain floating when $V_{GS} > V_{bi} > 0$.

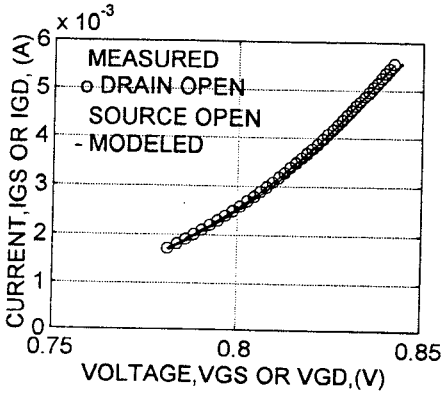

Fig. 3 Gate current I_{GS} or I_{GD} versus gate-source or gate-drain voltage at drain or source floating.

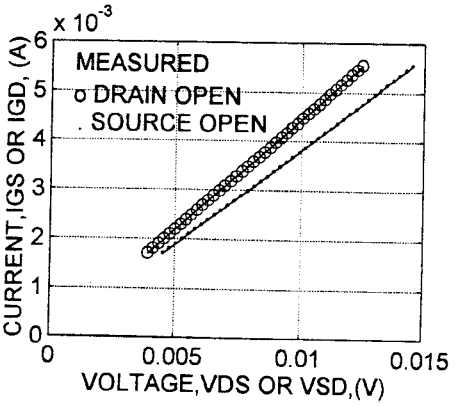

Fig. 4 Gate current I_{GS} or I_{GD} versus drain-source or source-drain voltage at drain or source floating when $V_{GS} > V_{bi} > 0$.

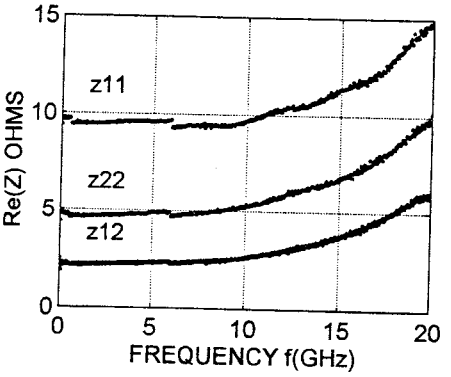

Fig. 5 Real part of Z_{ij} versus frequency at drain floating for $V_{GS} > V_{bi} > 0$.

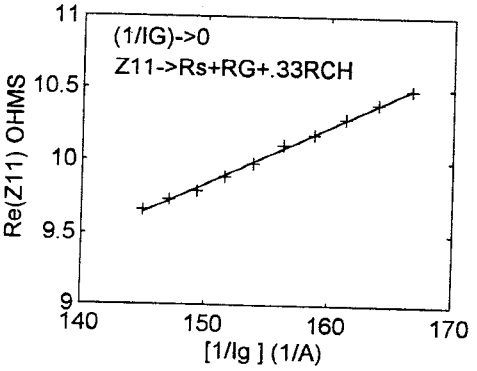

Fig. 6 Real part of Z_{11} versus $1/I_{GS}$ at drain floating for $V_{GS} > V_{bi} > 0$.